A NEW TECHNOLOGY FOR Si MICROWAVE POWER TRANSISTOR MANUFACTURING

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Abstract

We, for the first time, demonstrate a new process for Si power transistor manufacturing. The new process, combining the HMIC process and flip-chip process, completely changes the Si power transistor internal matching circuits design and manufacturing. S-band Si power transistor was used as a testing vehicle and under pulse operation condition Pout=23 W with 7.9 dB of gain and 39% of efficiency were obtained at f=3.05GHz and Vcc=36V.

I. Introduction

Si bipolar junction transistors (BJT) have been widely used for microwave applications, especially for high power amplification. Si power transistors, being widely used in the state-of-art military and commercial systems, are still manufactured using the technology developed 20 years ago. Due to its large emitter periphery a typical Si microwave power transistor has very low input impedance and large output capacitance. Thus the internal impedance matching circuits are required for most of the applications[1]. Fig. 1 shows a typical packaged Si microwave power transistor manufactured using the conventional process. Inside the ceramic package Si microwave power transistors are mounted onto an insulating substrate. Then chip capacitors and bonding wires are utilized to form the internal impedance matching circuits. Thus in order to get required inductance the length and shape of the bonding wires have to be tightly controlled and in many cases manual tuning is required by reshaping the bonding wires. Although this process has been widely used since then, it is, by its nature, a complex and labor intensive process. Further more, as a direct consequence of this process, an expensive BeO package is required to reduce the thermal resistance. Attempt had been made to change this manufacturing process. One approach was to integrate the impedance matching circuits and the Si BJT on one chip of silicon[2]. It was pursued without success because of the formidable RF loss caused by conductive Si substrates[3].

In this study a new manufacturing process[4] is proposed and demonstrated. In this new process, a Heterolithic Microwave Integrated Circuit

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(HMIC)[5] , developed at M/A-COM, is used as the integration medium for impedance matching circuits fabrication, while discrete Si microwave power transistors are seamless integrated into the impedance matching circuits by flip-chip process. Being completely different from the existing Si microwave power transistor design and manufacturing, the new process will not only reduce the manufacturing and package cost, but also improve the device performance and reliability. S-band Si microwave power transistor was chosen as a testing vehicle to demonstrate the

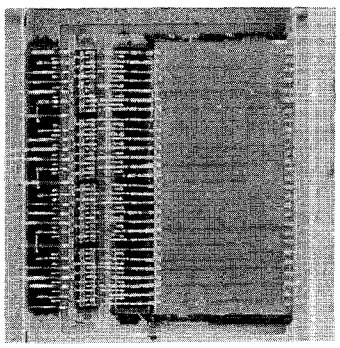

Fig.1 Si power transistor with internal matching circuits fabricated using conventional process. 4 transistors cell are shown in the package.

process. In pulse operation Pout=23 W with 7.9 dB of gain and 39% of efficiency were obtained at f=3.05GHz and Vcc=36V. And this performance was achieved in first design without any internal tuning.

II. Description of the new process

Basically, the new process utilizes the HMIC technology for impedance matching circuits fabrication and flip-chip technology for integrating the Si power transistor into HMIC circuit. Fig. 2 shows the schematic of an Si power transistor constructed by using the new process.

The HMIC technology, developed at M/A-COM, combines the properties of silicon and

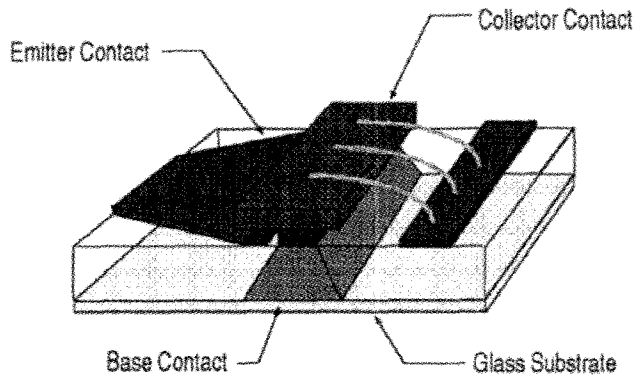

Fig. 2 The conceptual drawing shows the Si power transistor mounted onto the HMIC substrate. The input and output matching circuits are not shown.

glass to create low-loss circuits for RF/microwave applications. The basic substrate consists of silicon pedestals embedded in a glass medium. As shown in Fig. 2 the Si pedestals provide both electrical and thermal ground, which is vital for power applications. The glass, which has low dielectric constant (4.1) and low loss tangent (0.002@ 10GHz), provides electrical isolation and mechanical support. Since glass is an amorphous material, it can be polished to a fine surface finish. Hence it can readily support thin-film deposition and fine-line photolithographic processes. Batch processes can be used to fabricate passive circuit elements like spiral inductors, MIM capacitors and thin film resistors at low cost, high performance, and good reliability. The low loss tangent of glass allows the fabrication of high-Q passive elements. The nature of thin film process provides the HMIC technology having at least the same integration level as GaAs based MMIC technology.

The flip-chip technology, also developed at M/A-COM, accommodates both electrical and thermal requirements for Si microwave power transistor package. The bump metal consists of Au/Pt/Au:Sn multilayer structure. Au is chosen to form the major portion of the bump because of

its high electrical and thermal conductivities. The bump is designed to cover the entire active area on the Si BJT to maximize the thermal conduction path. Using the flip-chip process the emitter and base contacts are formed by short metal bumps. Thus the common mode inductance is virtually eliminated which improves the stability of the transistor.

To demonstrate this new manufacturing process, an S-band Si power transistor was chosen as the vehicle. The transistor was designed for broadband class C operation in common base configuration. The new manufacturing process consists of two steps: 1) the design and fabrication of the impedance matching circuit on HMIC substrate and 2) the Si power transistor mounting using flip-chip technology. As mentioned above, since the HMIC substrate supports the standard thin film processes, the design and fabrication of the impedance matching circuit are very much similar to the standard MMIC processes. HP Microwave-Design-System(MDS) was used for the input and output impedance matching circuit design. Since the large signal model of the Si power transistor was not available, the impedance matching circuits were designed around the estimated input and output impedance of the Si power transistor under large signal drive. The designed matching circuits were then realized on the HMIC substrate. The HMIC substrates were prepared using the standard HMIC process, which has been reported elsewhere[6]. The substrate height was 200 μm. Standard thin film processes were employed to fabricate the impedance matching circuit. The metal thickness for the passive elements is 7.5 μm to minimize the circuit resistive loss. The bumps on the Si power transistor were formed by a metal evaporation/lift-off procssses. The evaporation/lift-off processes not only provide a flat contact surface which is vital from the thermal point of view, but also assure simple fabrication processes. The metal bumps consists of Au/Pt/Au:Sn layers. Au forms the major portion of the bump. Since the bump is on top of the device active area, mechanical loading during the flip-chip bonding process should be minimized. Thus Au:Sn is selected as the top layer and the bonds between the transistor and the HMIC substrate are formed by eutectic bonding. Pt is the diffusion barrier between the Au and Au:Sn layers. As shown in Fig. 2, the emitter and base contacts were formed by flip-chip bonding and collector, which is on the backside of the device, was wired into the circuit using bonding wires. Fig. 3 depicts the finished Si power transistor. As shown in Fig. 3 all the matching circuits are formed by spiral inductors and MIM capacitors. The chip capacitors and bonding wires shown in Fig. 1 are eliminated.

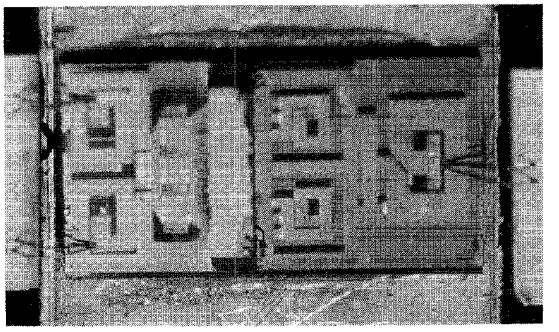

Fig. 3 The finished S-band Si power transistor with internal impedance matching circuit fabricated using the new manufacturing process.

III. Results and discussions

For RF power evaluation the finished transistor was mounted onto a Cu testing fixture. The input of the transistor was DC grounded by a RF choke to guarantee the class C operation. Fig. 4 depicts the power saturation characteristics of the finished power transistor. Without any internal tuning this performance was comparable to what the conventional Si power transistor manufacturing process can normally achieve. Comparing the Fig. 1 with Fig. 3, it is obvious that the new

Table 1 A comparison between the conventional process and the new process. The comparison is based on the same Si die with same power handling capability.

	New	Conventional
# of wire bonds	6 (No tuning)	>30 (Tuning required)
Matching circuit formation	Wafer level/batch mode fabrication	Package level/ wire bonding
Wafer level assembly	Yes	No
Wafer level testing	Yes	No
BeO package	Not required	Required

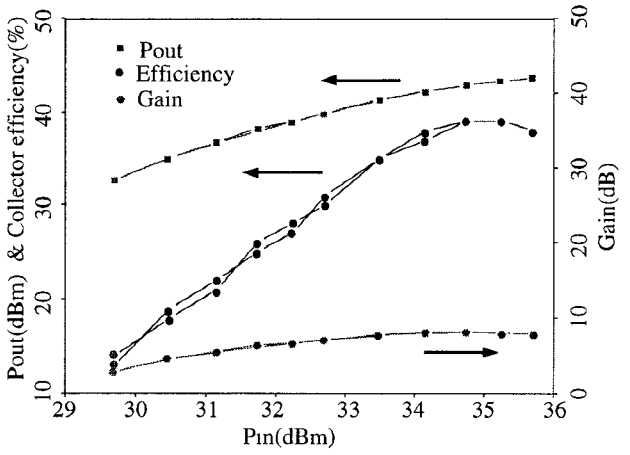

Fig. 4 The power saturation characteristic of Si power transistor made by new process. Vcc=36V, f=3.05 GHz, pulse width=10 μs, duty cycle=5%. Tuned for maximum output power.

process provides many manufacturing advantages. Table 1 summarizes the basic differencs between the conventional process and the new process.. It is clear that these manufacturing advantages will have profound impacts on cost reduction and performance enhancement of Si RF power transistors.

IV. Summary

In summary, a new process was proposed and demonstrated for Si microwave power transistor manufacturing. The new process, being completely from the existing conventional technology, will not only greatly improve the manufacturing but also enhance the performance of Si microwave power transistors. S-band Si power transistor was chosen as the demonstrating vehicle and under pulse operation condition Pout=23 W with 7.9 dB of gain and 39% of efficiency were obtained at f=3.05GHz and Vcc=36V.

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References

[1] Octavius Pitzalis, JR., and Russell Gilson, "Broadband microwave class-C transistor Amplifiers", IEEE Trans. Microwave Theory Tech., Vol. MTT-21, pp660-668, 1973.

[2] Richard Allison, "Silicon bipolar microwave power transistors", IEEE Trans. Microwave Theory Tech., Vol. MTT-27, pp415-422, 1979.

[3] T. M. Hyltin, "Microstrip transmission on semiconductor substrates", IEEE Trans. Microwave Theory Tech., Vol. MTT-13, pp777-781, 1965.

[4] Ping Li, "Method of impedance matching circuit making and substrate therefore", Patent filed.

[5] J. L. Goodrich and C. C. Souchuns, "Pin diode and method for making same", US Patent No 5268310, 1993.

[6] P. Chinoy, et al, "Manufacture of low-loss microwave circuits using HMIC technology", 1994 IEEE MTT-S Digest, pp1137-1140, 1994.